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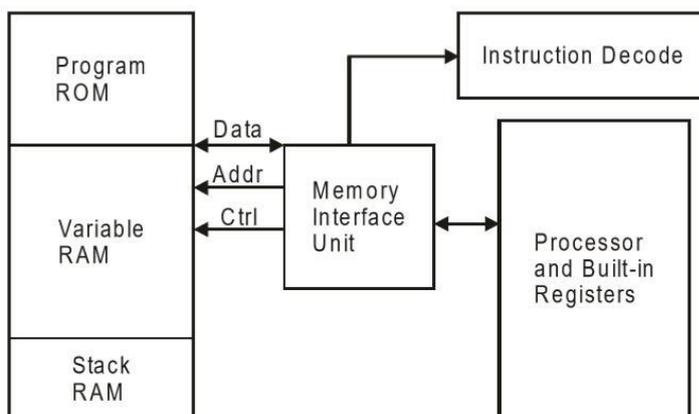
Unit: III

Topic: Embedded Systems Architecture

### **Von Neumann Architecture**

The Von Neumann architecture was first proposed by a computer scientist John von Neumann. In this architecture, one data path or bus exists for both instruction and data. As a result, the CPU does one operation at a time. It either fetches an instruction from memory, or performs read/write operation on data. So an instruction fetch and a data operation cannot occur simultaneously, sharing a common bus.

Memory space

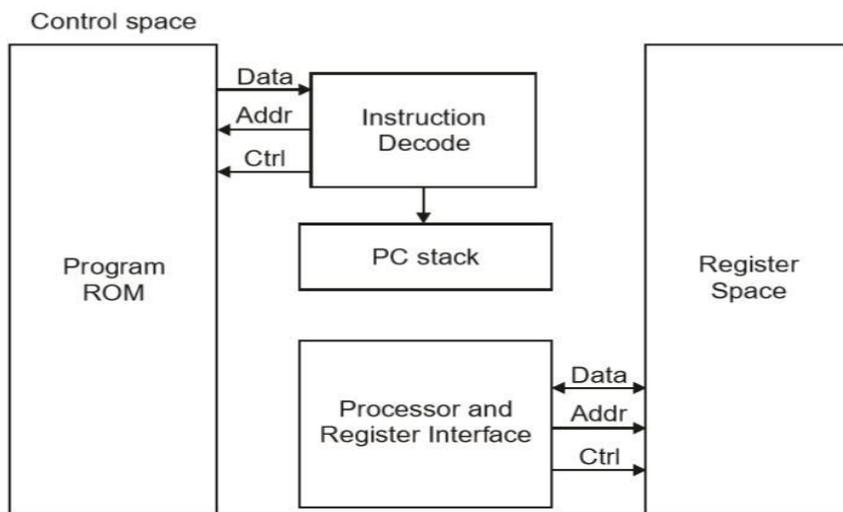


Von-Neumann architecture supports simple hardware. It allows the use of a single, sequential memory. Today's processing speeds vastly outpace memory access times, and we employ a very fast but small amount of memory (cache) local to the processor.

### Harvard Architecture

The Harvard architecture offers separate storage and signal buses for instructions and data. This architecture has data storage entirely contained within the CPU, and there is no access to the instruction storage as data. Computers have separate memory areas for program instructions and data using internal data buses, allowing simultaneous access to both instructions and data.

Programs needed to be loaded by an operator; the processor could not boot itself. In a Harvard architecture, there is no need to make the two memories share properties.



### Von-Neumann Architecture vs Harvard Architecture

The following points distinguish the Von Neumann Architecture from the Harvard Architecture:

<i>Point of comparison</i>	<i>Harvard architecture</i>	<i>Von Neumann Architecture</i>
Arrangement	In Harvard architecture, the CPU is connected with both the data memory (RAM) and program memory (ROM), separately.	In Von-Neumann architecture, there is no separate data and program memory. Instead, a single memory connection is given to the CPU.
Hardware requirements	It requires more hardware since it will be requiring separate data and address bus for each memory.	In contrast to the Harvard architecture, this requires less hardware since only a common memory needs to be reached
Space requirements	This requires more space.	Von-Neumann Architecture requires less space.

Speed of execution	Speed of execution is faster because the processor fetches data and instructions simultaneously .	Speed of execution is slower since it cannot fetch the data and instructions at the same time
Space usage	It results in wastage of space since if the space is left in the data memory then the instructions memory cannot use the space of the data memory and vice-versa.	Space is not wasted because the space of the data memory can be utilized by the instructions memory and vice-versa.
Controlling	Controlling becomes complex since data and instructions are to be fetched simultaneously.	Controlling becomes simpler since either data or instructions are to be fetched at a time.

### ISA (instruction set architecture:

The **instruction set**, also called **ISA (instruction set architecture)**, is part of a computer that pertains to programming, which is basically **machine language**. The instruction set provides commands to the processor, to tell it what it needs to do. The instruction set consists of addressing modes, instructions, native data types, registers, memory architecture, interrupt, and exception handling, and external **I/O**.

An example of an instruction set is the **x86 instruction set**, which is common to find on computers today. Different computer processors can use almost the same instruction set while still having very different internal design. Both the **Intel Pentium** and **AMD Athlon** processors use nearly the same **x86 instruction set**. An instruction set can be built into the hardware of the processor, or it can be emulated in software, using an interpreter. The hardware design is more efficient and faster for running programs than the emulated software version.

### Examples of instruction set

- **ADD** - Add two numbers together.
- **COMPARE** - Compare numbers.
- **IN** - Input information from a device, e.g.,  
 keyboard.
- **JUMP** - Jump to designated RAM address.
- **JUMP IF** - Conditional statement that jumps to a  
 designated RAM address.
- **LOAD** - Load information from RAM to the CPU.

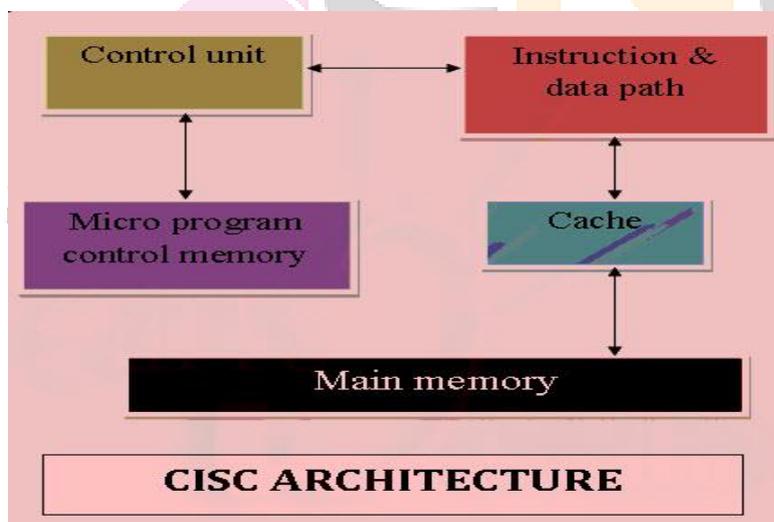
- **OUT** - Output information to device, e.g., monitor.
- **STORE** - Store information to RAM.

## RISC and CISC Architecture :

### CISC Architecture:

CISC Stands for "Complex Instruction Set Computing." This is a type of microprocessor design. The CISC architecture contains a large set of computer instructions that range from very simple to very complex and specialized. Though the design was intended to compute complex instructions in the most efficient way, it was later found that many small, short instructions could compute complex instructions more efficiently. This led to a design called Reduced Instruction Set Computing (RISC), which is now the other major kind of microprocessor architecture. Intel Pentium processors are mainly CISC-based, with some RISC facilities built into them, whereas the PowerPC processors are completely RISC-based.

The CISC approach attempts to minimize the number of instructions per program, sacrificing the number of cycles per instruction. Computers based on the CISC architecture are designed to decrease the memory cost. Because, the large programs need more storage, thus increasing the memory cost and large memory becomes more expensive. To solve these problems, the number of instructions per program can be reduced by embedding the number of operations in a single instruction, thereby making the instructions more complex.



### CISC Architecture

- MUL loads two values from the memory into separate registers in CISC.
- CISC uses minimum possible instructions by implementing hardware and executes operations.
- Instruction Set Architecture is a medium to permit communication between the programmer and the hardware. Data execution part, copying of data, deleting or editing is the user commands used in the microprocessor and with this microprocessor the Instruction set architecture is operated.
- The main keywords used in the above Instruction Set Architecture are as below

### CHARACTERISTIC OF CISC:-

1. Complex instruction, hence complex instruction decoding.
2. Instruction are larger than one word size.
3. Instruction may take more than single clock cycle to get executed.
4. Less number of general purpose register as operation get performed in memory itself.
5. Complex Addressing Modes.
6. More Data types.

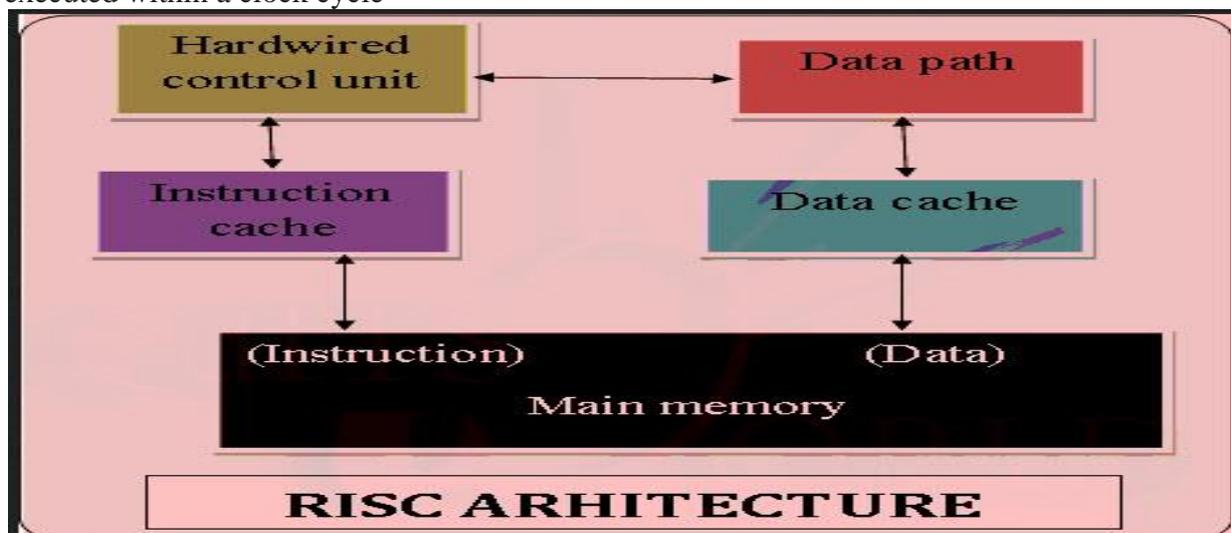
**Example** – Suppose we have to add two 8-bit number:

- **CISC approach:** There will be a single command or instruction for this like ADD which will perform the task.

### RISC Architecture:

RISC Stands for "Reduced Instruction Set Computing" and is pronounced "risk." RISC is a type of processor architecture that uses fewer and simpler instructions than a complex instruction set computing (CISC) processor. RISC processors perform complex instructions by combining several simpler ones.

Several CPUs in the 1990s and early 2000s used RISC architecture. One of the most popular was the IBM PowerPC processor, which Apple used in its PowerMac line of computers for nearly a decade. In 2006, Apple switched to CISC-based Intel CPUs. Nearly all personal computers now use CISC processors made by Intel or AMD. RISC (Reduced Instruction Set Computer) is used in portable devices due to its power efficiency. For Example, Apple iPod and Nintendo DS. RISC is a type of microprocessor architecture that uses highly-optimized set of instructions. RISC does the opposite, reducing the cycles per instruction at the cost of the number of instructions per program. Pipelining is one of the unique feature of RISC. It is performed by overlapping the execution of several instructions in a pipeline fashion. It has a high performance advantage over CISC. RISC processors take simple instructions and are executed within a clock cycle



RISC Architecture

### **Characteristic of RISC –**

1. Simpler instruction, hence simple instruction decoding.
2. Instruction come under size of one word.
3. Instruction take single clock cycle to get executed.
4. More number of general purpose register.
5. Simple Addressing Modes.
6. Less Data types.
7. Pipeling can be achieved.

**Example –** Suppose we have to add two 8-bit number:

- **RISC approach:** Here programmer will write first load command to load data in registers then it will use suitable operator and then it will store result in desired location.

### **The Advantages of RISC architecture:-**

- RISC(Reduced instruction set computing)architecture has a set of instructions, so high-level language compilers can produce more efficient code
  - It allows freedom of using the space on microprocessors because of its simplicity.
  - Many RISC processors use the registers for passing arguments and holding the local variables.
  - RISC functions use only a few parameters, and the RISC processors cannot use the call instructions, and therefore, use a fixed length instruction which is easy to pipeline.
  - The speed of the operation can be maximized and the execution time can be minimized.
- Very less number of instructional formats, a few numbers of instructions and a few addressing modes are needed.

### **The Disadvantages of RISC architecture:-**

- Mostly, the performance of the RISC processors depends on the programmer or compiler as the knowledge of the compiler plays a vital role while changing the CISC code to a RISC code
- While rearranging the CISC code to a RISC code, termed as a code expansion, will increase the size. And, the quality of this code expansion will again depend on the compiler, and also on the machine's instruction set.
- The first level cache of the RISC processors is also a disadvantage of the RISC, in which these processors have large memory caches on the chip itself. For feeding the instructions, they require very fast memory systems.

### **Advantages of CISC architecture:-**

- Microprogramming is easy assembly language to implement, and less expensive than hard wiring a control unit.
- The ease of microcoding new instructions allowed designers to make CISC machines upwardly compatible:
- As each instruction became more accomplished, fewer instructions could be used to implement a given task

**Disadvantages of CISC architecture:-**

- The performance of the machine slows down due to the amount of clock time taken by different instructions will be dissimilar
- Only 20% of the existing instructions is used in a typical programming event, even though there are various specialized instructions in reality which are not even used frequently.
- The conditional codes are set by the CISC instructions as a side effect of each instruction which takes time for this setting – and, as the subsequent instruction changes the condition code bits – so, the compiler has to examine the condition code bits before this happens.

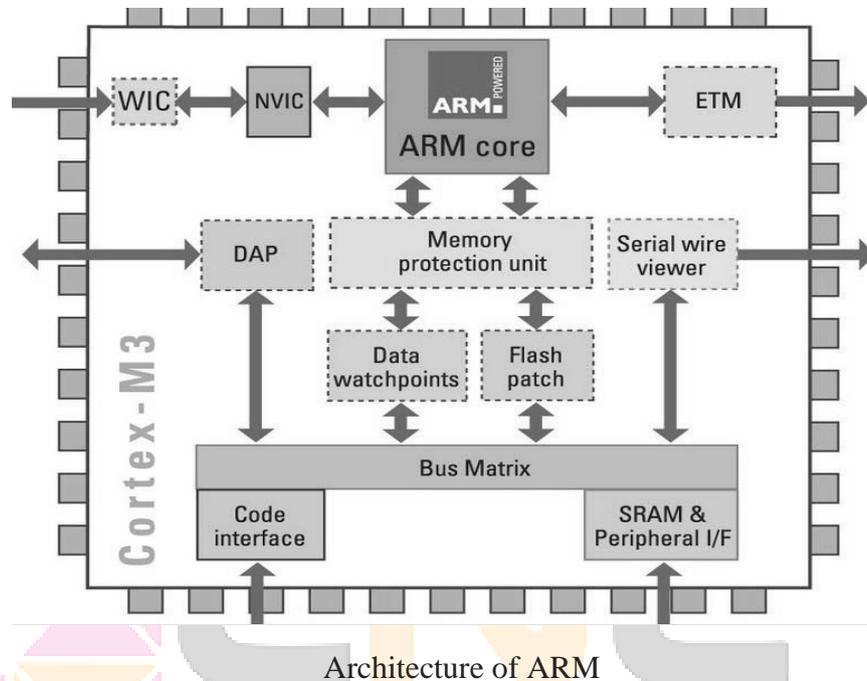
**CISC vs RISC**

- The following points differentiate a CISC from a RISC –

<b>CISC</b>	<b>RISC</b>
Larger set of instructions. Easy to program	Smaller set of Instructions. Difficult to program.
Simpler design of compiler, considering larger set of instructions.	Complex design of compiler.
Many addressing modes causing complex instruction formats.	Few addressing modes, fix instruction format.
Instruction length is variable.	Instruction length varies.
Higher clock cycles per second.	Low clock cycle per second.
Emphasis is on hardware.	Emphasis is on software.
Control unit implements large instruction set using micro-program unit.	Each instruction is to be executed by hardware.
Slower execution, as instructions are to be read from memory and decoded by the decoder unit.	Faster execution, as each instruction is to be executed by hardware.
Pipelining is not possible.	Pipelining of instructions is possible, considering single clock cycle.

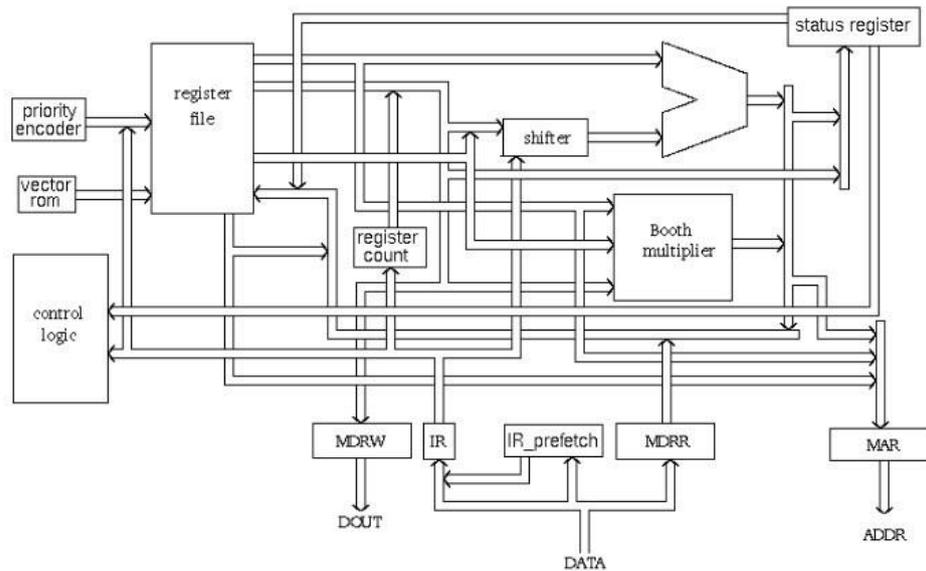
## ARM Processor:

The ARM architecture processor is an advanced reduced instruction set computing [RISC] machine and it's a 32bit reduced instruction set computer (RISC) microcontroller. This ARM is a family of microcontroller developed by makers like ST Microelectronics, Motorola. The ARM architecture comes with totally different versions like ARMv1, ARMv2, etc.



The ARM Architecture consists of:

- Arithmetic Logic Unit
- Booth multiplier
- Barrel shifter
- Control unit
- Register file



Block diagram of ARM

### Arithmetic Logic Unit (ALU):

The ALU has two 32-bit inputs. The primary comes from the register file, whereas the other comes from the shifter. Status registers flags modified by the ALU outputs. The V-bit output goes to the V flag as well as the Count goes to the C flag. Whereas the foremost significant bit really represents the S flag, the ALU output operation is done by NO Red to get the Z flag. The ALU has a 4-bit function bus that permits up to 16 opcodes to be implemented.

### Booth Multiplier Factor:

The multiplier factor has 3 32-bit inputs and the inputs return from the register file. The multiplier output is barely 32-Least Significant Bits of the merchandise. The entity representation of the multiplier factor is shown in the above block diagram. The multiplication starts whenever the beginning 04 input goes active. Fin of the output goes high when finishing.

### Booth Algorithm

Booth algorithm is a noteworthy multiplication algorithmic rule for 2's complement numbers. This treats positive and negative numbers uniformly. Moreover, the runs of 0's or 1's within the multiplier factor are skipped over without any addition or subtraction being performed, thereby creating possible quicker multiplication. The figure shows the simulation results for the multiplier test bench. It's clear that the multiplication finishes only in 16 clock cycle.

The barrel shifter features a 32-bit input to be shifted. This input is coming back from the register file or it might be immediate data. The shifter has different control inputs coming back from the instruction register. The Shift field within the instruction controls the operation of the barrel shifter. This field indicates the kind of shift to be performed (logical left or right, arithmetic right or rotate right). The quantity by which the register ought to be shifted is contained in an immediate field within the instruction or it might be the lower 6 bits of a register within the register file.

### **Digital Signal Processors (DSP):**

**Digital Signal Processor (DSP)** is actually a special-purpose CPU used for digital signal processing-based applications. Once a signal is converted into digital data, using multiple different available algorithms (such as Fast Fourier Transform), its components can be isolated, analyzed and rearranged more easily than in analogue form. It provides ultrafast instruction sequences, such as shift and add, and multiply and add, which are commonly used in math intensive signal processing. DSP is having versatile application in multiple different fields, including biomedicine, sonar, radar, seismology, cell phones, fax machines, audio, digital TV, sound cards, modems, hard disks, imaging and communications, speech and music processing. It can also be used to create the concert hall and along with surround sound effects in stereo and home theatre equipment.

Digital Signal Processors (DSPs) have following characteristics:

- a) Real-time digital signal processing capabilities. DSPs typically have to process data in real time, i.e., the correctness of the operation depends heavily on the time when the data processing is completed.
- b) High throughput: DSPs can sustain processing of high-speed streaming data, such as audio and multimedia data processing.
- c) Deterministic operation: The execution time of DSP programs can be foreseen accurately, thus guaranteeing a repeatable, desired performance.
- d) Re-programmability by software: Different system behavior might be obtained by re-coding the algorithm executed by the DSP instead of by hardware modifications.

Example:

1. TMS320C54X from Texas instruments.
2. SHARC of analog device
3. 5600XX OF Motorola